

tion does not go through the intermediate step of Ni_2GaAs formation, since Ni interfaces the substrate only at relatively high temperatures when this ternary compound is already unstable. Similarly, for the alloy film of $\text{Ni}_{60}\text{Ta}_{40}$, some amount of Ni leaches out of the alloy to form Ni_2GaAs at temperatures lower than 500°C . At the range of temperatures of $500\text{--}600^\circ\text{C}$ as can already be expected from the bilayer samples, we obtain $\text{NiTaAs}/\text{NiGa}/\text{GaAs}$; and finally at higher temperatures and long heat treatments NiTaAs will also dissociate to NiGa and TaAs . All three schemes of Ni-Ta metallization (Ni-Ta, Ni/Ta, and Ta/Ni) resulted after the heat treatment of 1 h at 600°C in a similar structure, namely, $\text{TaAs}(\text{Ni})/\text{NiGa}/\text{GaAs}$. Thus it is clearly seen that there is some driving force for Ni to reach the interface with GaAs and to form there epitaxially the compound of NiGa . This probably is because of a gain in the free energy due to epitaxial compound formation.

From the practical point of view two schemes are interesting. The bilayer of Ta/Ni on GaAs, or any other refractory metal/transition metal on GaAs, provides a metal which reacts easily with the substrates and determines the electrical properties of the contact, and a top layer which is inert at low temperatures and can serve as a diffusion barrier to the outermost metallization of Au or Al. The second attractive scheme is the alloy of a near noble and a refractory metal. At temperatures in the range between the reaction temperatures of both metals on GaAs we find, similarly to the situation on Si, a near-noble metal compound at the innermost part of the contact and the unreacted alloy at the outer part. The first layer may form a shallow contact, since the substrate consumption is limited by the concentration of the near-noble metal in the alloy film; the outer layer can

serve as a built-in diffusion barrier. Certainly compositions rich in the refractory metal are preferred for this application. Thus, although an alloy film on GaAs behaves in a more complicated way than on Si, at least from the metallurgical point of view it results in quite similar structures. Potential device applications certainly depend on the electrical characteristics of the metallization/GaAs interface which have not yet been explored.

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- ¹K. N. Tu and J. W. Mayer, in *Thin Films—Interdiffusion and Reactions*, edited by J. M. Poate, K. N. Tu, and J. W. Mayer (Wiley, New York, 1978), Chap. 10.
- ²S. P. Murarka *Silicides for VLSI Applications* (Academic, New York, 1983).
- ³J. O. Olowolafe, K. N. Tu, and J. Angilello, *J. Appl. Phys.* **50**, 6316 (1979).
- ⁴J. W. Mayer, S. S. Lau, and K. N. Tu, *J. Appl. Phys.* **50**, 5855 (1979).
- ⁵K. N. Tu, W. N. Hammer, and J. O. Olowolafe, *J. Appl. Phys.* **51**, 1663 (1980).
- ⁶G. Ottaviani, K. N. Tu, J. W. Mayer, and B.-Y. Tsaur, *Appl. Phys. Lett.* **36**, 1331 (1980).
- ⁷M. Eizenberg and K. N. Tu, *J. Appl. Phys.* **53**, 1577 (1983).
- ⁸M. Ogawa, *Thin Solid Films* **70**, 181 (1980).
- ⁹A. Lahav, Ph. D. thesis, Technion-Israel Institute of Technology (to be published).
- ¹⁰J. O. Olowolafe, P. S. Ho, H. J. Hovel, J. E. Lewis, and J. M. Woodall, *J. Appl. Phys.* **50**, 955 (1979).
- ¹¹Y. A. Oustry, M. Caumont, A. Escant, A. Martinez, and B. Toprasertpong, *Thin Solid Films* **79**, 251 (1981).
- ¹²X. F. Zeng and D. D. L. Chung, *J. Vac. Sci. Technol.* **21**, 611 (1982).
- ¹³A. K. Sinha and J. M. Poate, in *Thin Films—Interdiffusion and Reactions*, edited by J. M. Poate, K. N. Tu, and J. W. Mayer (Wiley, New York, 1978), Chap. 11.
- ¹⁴C. Fontaine, T. Okumura, and K. N. Tu, *J. Appl. Phys.* **54**, 1404 (1983).

Vertical field-effect transistors in III-V semiconductors

Z. Rav-Noy, L.-T. Lu, E. Kapon, S. Mukai,^{a)} S. Margalit, and A. Yariv
California Institute of Technology, Pasadena, California 91125

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Vertical metal-semiconductor field-effect transistors in GaAs/GaAlAs and vertical metal-oxide-semiconductor field-effect transistors (MOSFET's) in InP/GaInPAs materials have been fabricated. These structures make possible short channel devices with gate lengths defined by epitaxy rather than by submicron photolithography processes. Devices with transconductances as high as 280 mS/mm in GaAs and 60 mS/mm (with 100-nm gate oxide) for the InP/GaInPAs MOSFET's were observed.

The introduction of double-diffused metal-oxide-semiconductor (DMOS) and vertical or V-groove metal-oxide-semiconductor (VMOS) based on silicon has led to significant improvements in the performance of microwave amplifiers, high-speed logic devices, and especially high vol-

tage switching devices.¹ III-V semiconductor devices offer superior performance due to the high electron mobility and saturation velocity. The vertical layered field-effect transistors (FET's) which are described in what follows, when combined with fine line lithography, can offer an attractive approach to the problem of extending transistor performance into the millimeter wave region. Another potential advan-

^{a)} Electrotechnical Laboratory, Ibaraki, Japan.

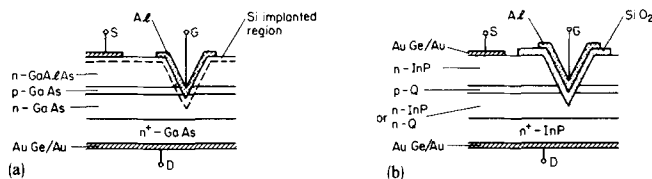


FIG. 1. (a) Schematic drawing of GaAs/GaAlAs vertical MESFET. (b) Schematic drawing of vertical InP/GaInPAs inversion mode MOSFET.

tage of such structures is in the field of power transistors. In these devices an important parameter is the on resistance which may be about six times smaller than in silicon. In the present work we demonstrate the feasibility of fabrication of submicron channels without submicron lithographic processes.

Vertical FET's were fabricated in GaAs/GaAlAs. The structure is shown in Fig. 1(a). The epitaxial layers were grown successively by liquid phase epitaxy (LPE) on n^+ -GaAs substrate with the following composition: $3\text{ }\mu\text{m}$ n -GaAs ($1.5 \times 10^{17}\text{ cm}^{-3}$), $0.15\text{ }\mu\text{m}$ p -GaAs ($1.2 \times 10^{17}\text{ cm}^{-3}$), $1.5\text{ }\mu\text{m}$ n -Ga_{0.8}Al_{0.2}As ($3 \times 10^{17}\text{ cm}^{-3}$). Grooves of $2.5\text{ }\mu\text{m}$ depth were etched. $6 \times 10^{12}\text{ cm}^{-2}$ Si was ion implanted at an energy of 120 keV. Annealing was performed with Si₃N₄ cap at 850 °C. Drain and source metalization is AuGe/Au and the gate is aluminum. Schottky diode breakdown voltage of $\sim 4\text{ V}$ and source resistance of $\sim 1\text{ }\Omega/\text{mm}$ were obtained.

The dc drain current-voltage characteristics of the device shown in Fig. 1(a) are shown in Fig. 2. A typical measured g_m value is about 250 mS/mm, the highest obtained is 280 mS/mm. A conservative correction for the source resistance yields values of intrinsic g_m as high as 320 mS/mm.

Vertical inversion mode MOSFET's in InP/InGaAsP were fabricated as shown in Fig. 1(b). The epitaxial layers were grown by LPE on n^+ -InP substrate with the following composition: $3\text{ }\mu\text{m}$ n -InP ($5 \times 10^{17}\text{ cm}^{-3}$), $0.3\text{ }\mu\text{m}$ p -Ga_{0.3642}In_{0.6358}P_{0.2}As_{0.8} ($2 \times 10^{17}\text{ cm}^{-3}$), $1.5\text{ }\mu\text{m}$ n -InP ($3 \times 10^{17}\text{ cm}^{-3}$). Grooves of $2\text{ }\mu\text{m}$ depths were etched and 100 nm SiO₂ is deposited by a silane chemical vapor deposition (CVD) reaction at 450 °C. AuGe/Au is defined and alloyed at 400 °C for 20 s for the drain and source. Finally Al is defined for the gate.

In Fig. 3 the dc drain current voltage characteristics of the device described in Fig. 1(b) are given. As shown in Fig. 3, the devices have nearly zero threshold voltage. A typical g_m value is about 50 mS/mm. The highest obtained is 60

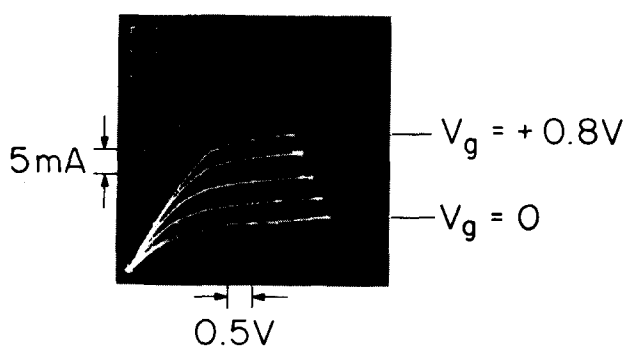


FIG. 2. Drain current-voltage characteristics of the GaAs/GaAlAs MESFET.

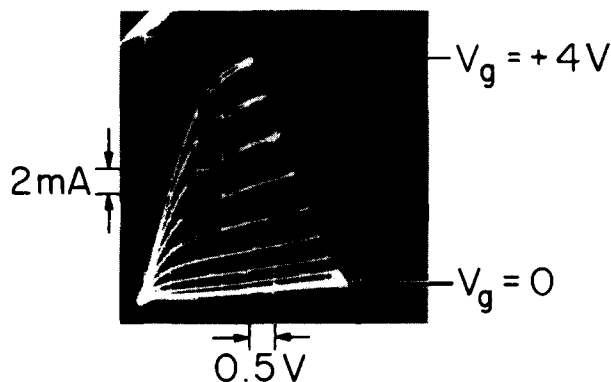


FIG. 3. Drain current-voltage characteristics of the InP/GaInPAs MOSFET.

mS/mm. This could be probably further improved by reducing the oxide thickness.² The MOSFET's suffered from severe hysteresis which indicates the existence of surface states. This could also contribute to lower dc transconductance. Optimization of the oxide might result in improved performance. We also did some preliminary experiments in asymmetric devices. We fabricated a device with heterosource (InP source, quaternary channel, and drain). When the device was operated in its normal mode (heterosource), the g_m values were 20% larger than in the reverse mode (heterodrain).

In a short channel InP/InGaAsP MOSFET there exists a practical and important limitation on the doping levels. To eliminate the undesirable source-drain punchthrough effect, the doping level in the p channel has to be high. In our case, we used $1\text{--}2 \times 10^{17}\text{ cm}^{-3}$ for the layer doping. It is possible to eliminate punchthrough effects by growing a voltage-supporting lightly doped drain.

The critical dimension in our devices is defined by the thickness of the epitaxially grown p layer and can thus be controlled to a degree of accuracy unattainable in lithographic processes, especially with advanced crystal growth techniques such as molecular beam epitaxy and metalorganic chemical vapor deposition. An advantage of vertical FET's is the ability to independently optimize the doping densities of the layers. In addition, the III-V material offers an extra degree of freedom unavailable in Si through the use of heterojunctions. The band discontinuity at heterojunction can be used to exploit transient electron transport phenomena such as velocity overshoot^{3,4} and ballistic transport⁵ to achieve high electron velocity. Moreover, the difference in mobility and band gap of III-V compounds can be utilized to optimize important parameters such as breakdown voltages in different applications.

We also note that a vertical FET in InP/InGaAsP materials is potentially interesting for microwave application because of the larger saturation velocity compared to GaAs. (The ternary alloy has also a higher mobility.) Also the reported structure [Fig. 1(b)] might be suitable for integration with $1.3\text{--}1.55\text{ }\mu\text{m}$ lasers and photodetectors which use the same material.

In conclusion, high transconductance vertical FET's have been fabricated in GaAs/GaAlAs and in InP/GaInPAs. The use of vertical structure makes possible submicron

devices which are fabricated without submicron photolithography. It is possible to embed a relatively thick and highly doped layer in close proximity to the gate. Transconductances of 280 mS/mm were obtained in GaAs/GaAlAs and 60 mS/mm in InP/InGaPAs. The full realization of the potential of these devices involves the use of fine line lithography in the lateral direction to reduce parasitics.

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¹C. Andre, T. Salama, and J. G. Oakes, IEEE Trans. Electron Devices **ED-25**, 1222 (1978).

²T. Itoh and K. Ohata, IEEE Trans. Electron Devices **ED-30**, 7 (1983).

³J. Y. Tang and K. Hess, IEEE Trans. Electron Devices **ED-29**, 1906 (1982).

⁴K. Tomizawa, Y. Awano, N. Hashirume, and M. Marashima, Electron. Lett. **19**, 1067 (1983).

⁵L. F. Eastman, R. Stall, D. Woodard, N. Dandaker, C. E. C. Wood, M. S. Shur, and K. Board, Electron. Lett. **16**, 524 (1980).

Space-charge-induced optoelectronic switching in IIa diamond

J. Glinski, X.-J. Gu, R. F. Code, and H. M. van Driel

Department of Physics and Erindale College, University of Toronto, Toronto, Canada M5S 1A7

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Experimental results are presented concerning the effect of contacts on the performance of high-voltage optoelectronic switching in insulating diamond. For high bias voltages and low intensity 222-nm, ≈ 7 -ns pulse illumination near the cathode, the switched voltage pulse splits into two peaks. The first peak corresponds to the high-speed photoconductive response of the diamond, while the second peak (which can be delayed up to ≈ 200 ns later) is attributed to space-charge-induced switching in the vicinity of the cathode.

Ultrafast optoelectronic switching has attracted considerable attention during the past few years.¹⁻³ Jitter-free operation and ultrafast rise time together with high-voltage handling capabilities make optoelectronic switches superior in comparison with electrical ones, especially when precise triggering of Pockels cells or streak cameras is required. One of the main limitations of switching materials studied to date is the maximum dc bias attainable, usually limited to a few kilovolts because of a thermal runaway effect. This problem can be reduced by using a wide-band-gap semiconductor with a high dielectric breakdown field.

In an earlier communication, Bharadwaj *et al.*⁴ reported high-voltage optoelectronic switching in IIa diamond which proved to be a high performance subnanosecond optoelectronic switch. However, the mechanism of switching has not been completely understood as yet. The elucidation of the mutual relationship between all major processes taking part in switching is important not only with regard to the particular application, but also with respect to improving the understanding of transient photoconductivity in insulating media. In this letter we report an interesting phenomenon discovered during experiments aimed at evaluating the influence of contacts on the switching characteristics.

The experimental setup and IIa diamond samples were the same as in Ref. 4. The photoconductivity of a 3-mm-long IIa diamond with Ti/Pt/Au electrodes was induced by ≈ 7 -ns pulses of 222-nm (5.58 eV) laser radiation from a Lumonics TE-860-2 KrCl excimer laser. However, instead of full illumination as was used in Ref. 4, the diamond was masked

so that only a 1-mm-wide region close to the negative electrode was illuminated. When the light intensity was 0.5 MW/cm² and the applied voltage was above 2 kV, the photoconductivity pulse split into two parts: the first one (P1) which has basically the same shape and time dependence as the light pulse and the second one (P2) which has a moderately fast rise time ≈ 10 ns, but a slower decay time of ≈ 100 –200 ns. Figure 1 shows a representative sequence of photoconductivity pulses observed with a Tektronix model 7912AD programmable digitizer.

When the light intensity and applied voltage are such that P1 and P2 are well separated, the main features of the observed behavior can be summarized as follows:

(1) With gradually decreasing laser pulse intensity: (a) the time separation between P1 and P2 increases; (b) when the time separation between P1 and P2 exceeds 40 ns, the appearance of P2 becomes more random in time with P2 being delayed with respect to P1 by an amount varying between ≈ 40 to ≈ 200 ns; (c) while the amplitude of P1 remains approximately constant at constant incident laser pulse intensity, both the amplitude and shape of P2 become less reproducible, especially when the time separation between P1 and P2 is greater than ≈ 40 ns; (d) the amplitude of P2 decreases much faster than that of P1 (as the laser intensity decreases) up to the point where P2 does not occur after every light pulse; even then, P2 can suddenly reappear after a number of laser excitation pulses (our repetition rate was ≈ 1 Hz).

(2) The character of the voltage dependence of the am-